REMARKS

I. Introduction

Claims 1 to 7 and 12 to 30 are currently pending and being considered in the present application. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

II. Rejection of Claims 1 to 7 and 12 to 30 Under 35 U.S.C. § 112

Claims 1 to 7 and 12 to 30 were rejected under 35 U.S.C. § 112, ¶ 2 as assertedly indefinite. The rejection should be withdrawn for the following reasons.

With respect to the assertions in the Office Action regarding claims 1, 2, 5 to 7, and 26, while Applicants do not agree with the merits of the rejection, nevertheless, to facilitate matters, the claims have been amended herein without prejudice for clarity to obviate the present rejection with respect to those claims.

As for claim 3, it is not apparent what the Examiner considers to be unclear. The claim clearly further defines a transferring step as including a step of inserting data into, and/or extracting data from, a data path. Accordingly, no amendment is necessary.

Withdrawal of the present indefiniteness rejection of claims 1 to 7 and 12 to 30 is therefore respectfully requested.

III. Rejection of Claims 1 to 7 and 12 to 30 Under 35 U.S.C. § 112

Claims 1 to 7 and 12 to 30 were rejected under 35 U.S.C. § 102 as assertedly anticipated by U.S. Patent No. 4,967,340 ("the Dawes reference"). The Dawes reference does not anticipate the present claims, and the rejection should be withdrawn, for at least the following reason.

Claim 1 relates to a method of processing data and recites, inter alia, that "an array . . . comprising a plurality of data processing cells that are configurable in their function . . . is coupled to the instruction pipeline [of at least one unit adapted for processing data in a sequential manner]." As is well understood by one of ordinary skill in the art, an instruction pipeline refers to a number of phases over which instructions are distributed, such that a number of instructions can be implemented simultaneously at different respective stages. Any review of the Dawes reference makes plain that it does not disclose, or even suggest, this feature.

The Office Action refers generally to an asserted coupling between elements 48 and 28 of the Dawes reference as assertedly disclosing the coupling of the array to the instruction pipeline. However, while the Dawes reference indicates that a CPU 48 and compiler 46 may form a configuration controller for configuring the random access processor 28, the Dawes reference makes no reference to an instruction pipeline, and certainly does not disclose, or even suggest, that the random access processor 28 may be coupled to an instruction pipeline of the CPU 48. The mere transmittal of instructions does not disclose an instruction pipeline.

Thus, the Dawes reference does not disclose, or even suggest, all of the features of claim 1, so that the Dawes reference does not anticipate claim 1 or any of its dependent claims 2 to 4 and 12 to 20.

As further regards claim 2, claim 2 provides that at least one data path is provided between the array and the at least one unit and includes a FIFO. The Office Action refers to the Abstract and column 5, lines 27 to 64 of the Dawes reference as assertedly disclosing this feature. However, the cited sections do not refer to memory of any kind between the CPU 48 and the random access processor 28 (referred to by the Office Action as assertedly disclosing the at least one unit and the array, respectively), let alone a FIFO. Indeed, any review of the Dawes reference makes plain that it does not at all disclose, or even suggest, a FIFO.

Moreover, claim 2 has been amended herein without prejudice to clarify the transferring step to include a transfer from the at least one unit to the array and vice versa. In contrast to claim 2, the Dawes reference provides for processing to be performed only by the random access processor 28. The CPU 48 is used merely to configure the random access processor 28. No data is indicated to be transferred from the random access processor 28 to the CPU 48.

For at least these additional reason, the Dawes reference does not disclose, or even suggest, all of the features of claim 2, so that the Dawes reference does not anticipate claim 2 for these additional reasons.

Each of independent claims 5 and 7 includes subject matter analogous to that of claim 1 discussed above in support of the patentability of claim 1, so that claims 5 (and its dependent claims 6 and 21 to 28) and claim 7 (and its dependent claims 29 and 30) are allowable for at least the same reasons set for the above in support of the patentability of claim 1.

As further regards claim 22, the claim has been amended herein without prejudice to recite that the array includes a runtime reconfigurable data processor. While the switches of the random access processor 28 of the Dawes reference are reconfigurable, nowhere does the Dawes reference disclose, or even suggest, that such reconfiguration may be at runtime. For this additional reason, the Dawes reference does not disclose, or even suggest, all of the features of claim 22, so that the Dawes reference does not anticipate claim 22 for this additional reason.

Withdrawal of this anticipation rejection of claims 1 to 7 and 12 to 30 is therefore respectfully requested.

IV. Conclusion

In light of the foregoing, it is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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